IN THE CLAIMS

None of the claims has been amended. However, a complete set of the pending claims is reproduced below for convenient reference by the Examiner, as follows:

1-54. (Canceled)

55. (Previously Presented) A memory device comprising:

a memory array including a number of memory cells;

an even row decoder located on a first side of the memory array;

an odd row decoder located on a second side of the memory array;

a single column decoder connected to the memory array;

a number of parallel wordlines local to the memory array coupled to gate regions of memory cells, including one or more even wordlines coupled to the even row decoder, and one or more odd wordlines coupled to the odd row decoder, the odd wordlines arranged alternately with the even wordlines; and

a number of strapping lines having lower resistance than the wordlines and connected to bypass portions of the wordlines within the memory array, wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder.

56. (Previously Presented) The memory device of claim 55, wherein the even row decoder is located directly adjacent the first side and the odd row decoder is located directly adjacent the second side.

57. (Previously Presented)The memory device of claim 55, wherein a strapping line connected to an odd wordline bypasses only one half of the wordline within the memory array nearer the odd row decoder and a strapping line connected to an even wordline bypasses only one half of the wordline within the memory array nearer the even row decoder.